FIG_1

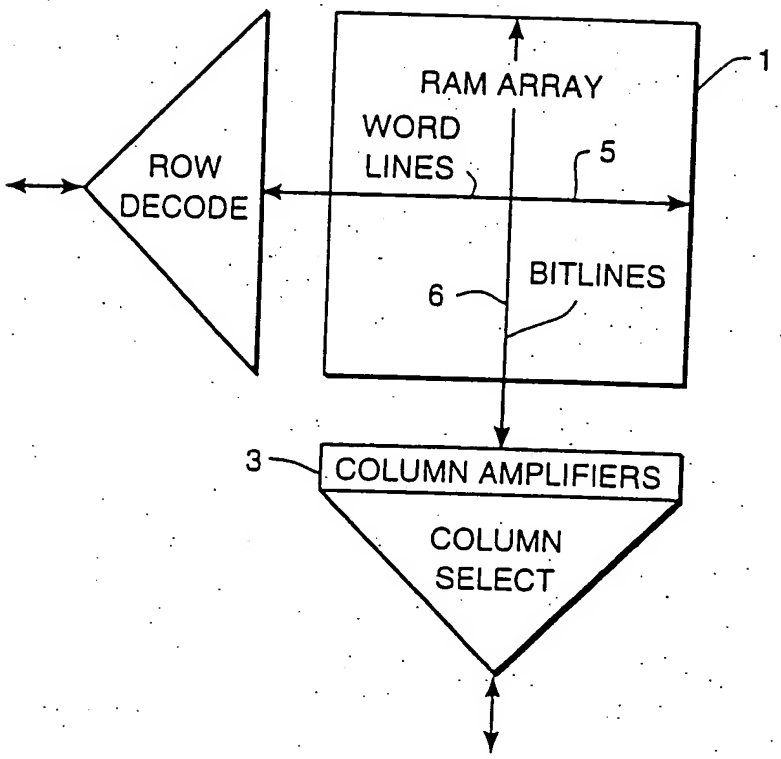

RAM ARRAY
1
WORD
LINES
5
ROW
DECODE
BITLINES
6
3
COLUMN AMPLIFIERS
COLUMN
SELECT

FIG_2

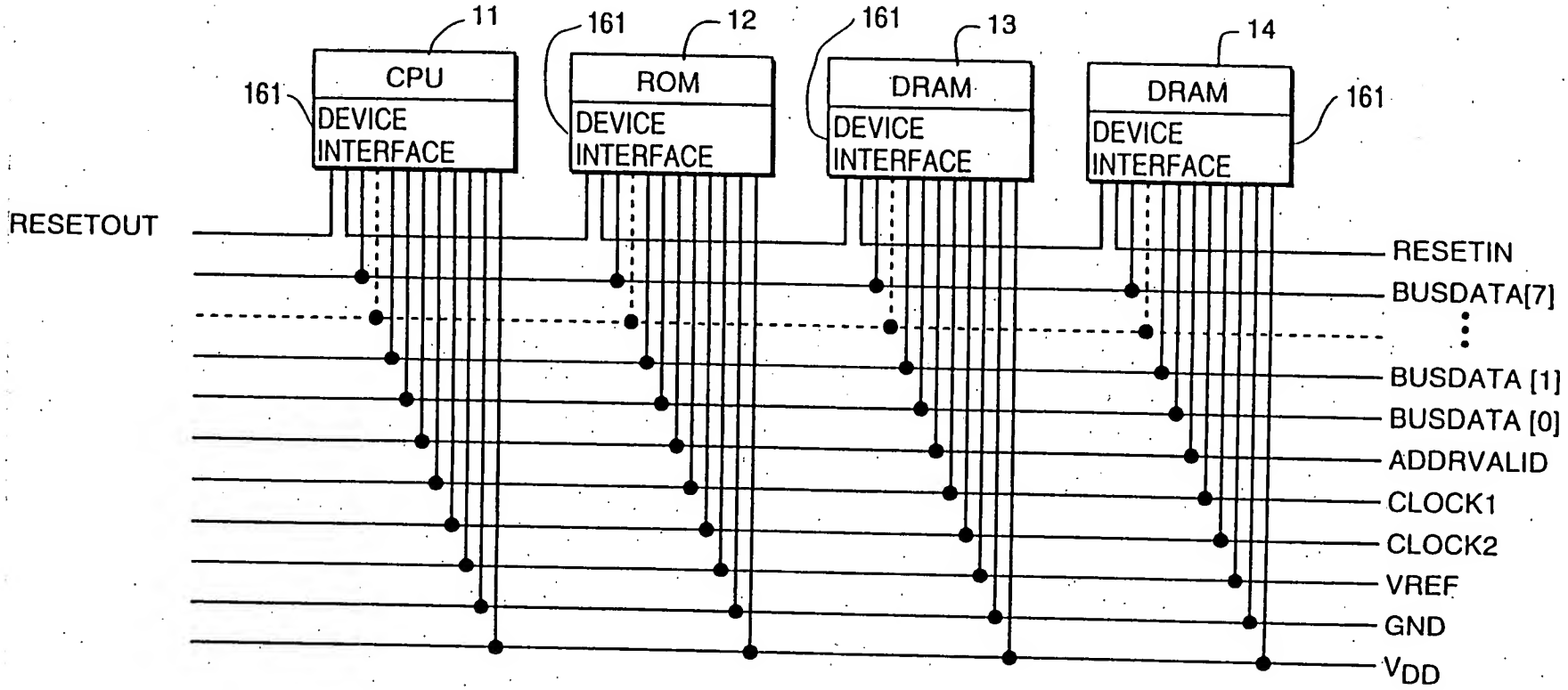
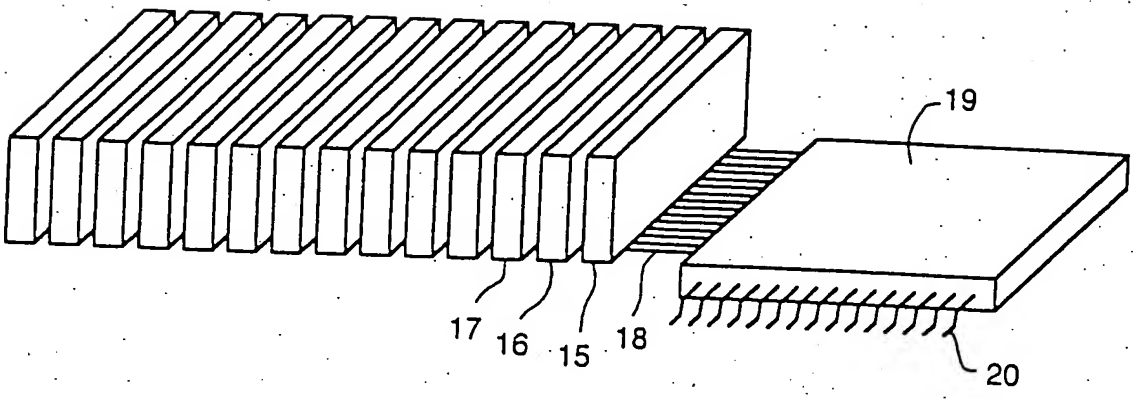

11
161
12
161
13
14
161
161
CPU
ROM
DRAM
DRAM
DEVICE INTERFACE
DEVICE INTERFACE
DEVICE INTERFACE
DEVICE INTERFACE
RESETOUT
RESETIN
BUSDATA[7]
BUSDATA [1]
BUSDATA [0]
ADDRVALID
CLOCK1
CLOCK2
VREF
GND
VDD

FIG_3



REGULAR ACCESS

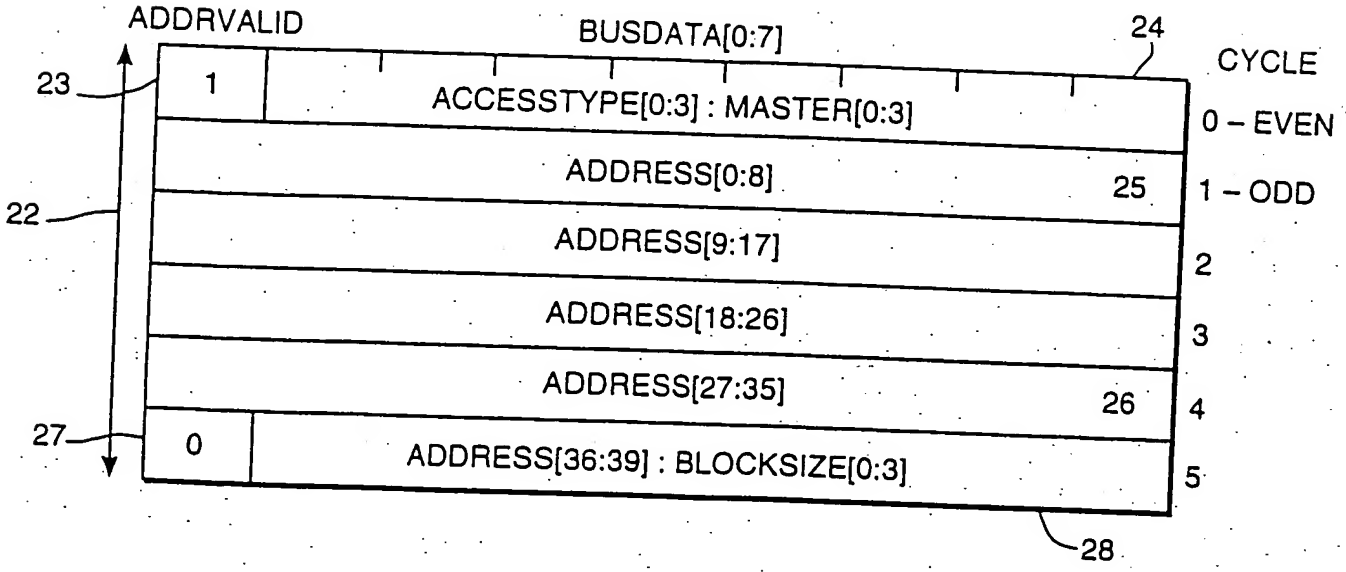


FIG_4

REJECT (NACK) CONTROL PACKET

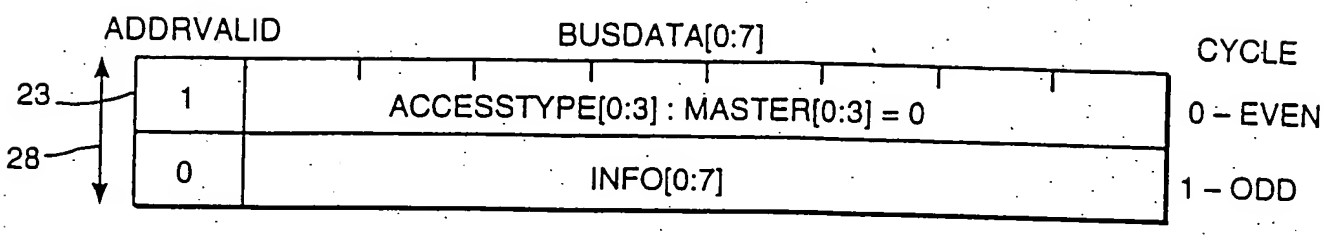


FIG_5

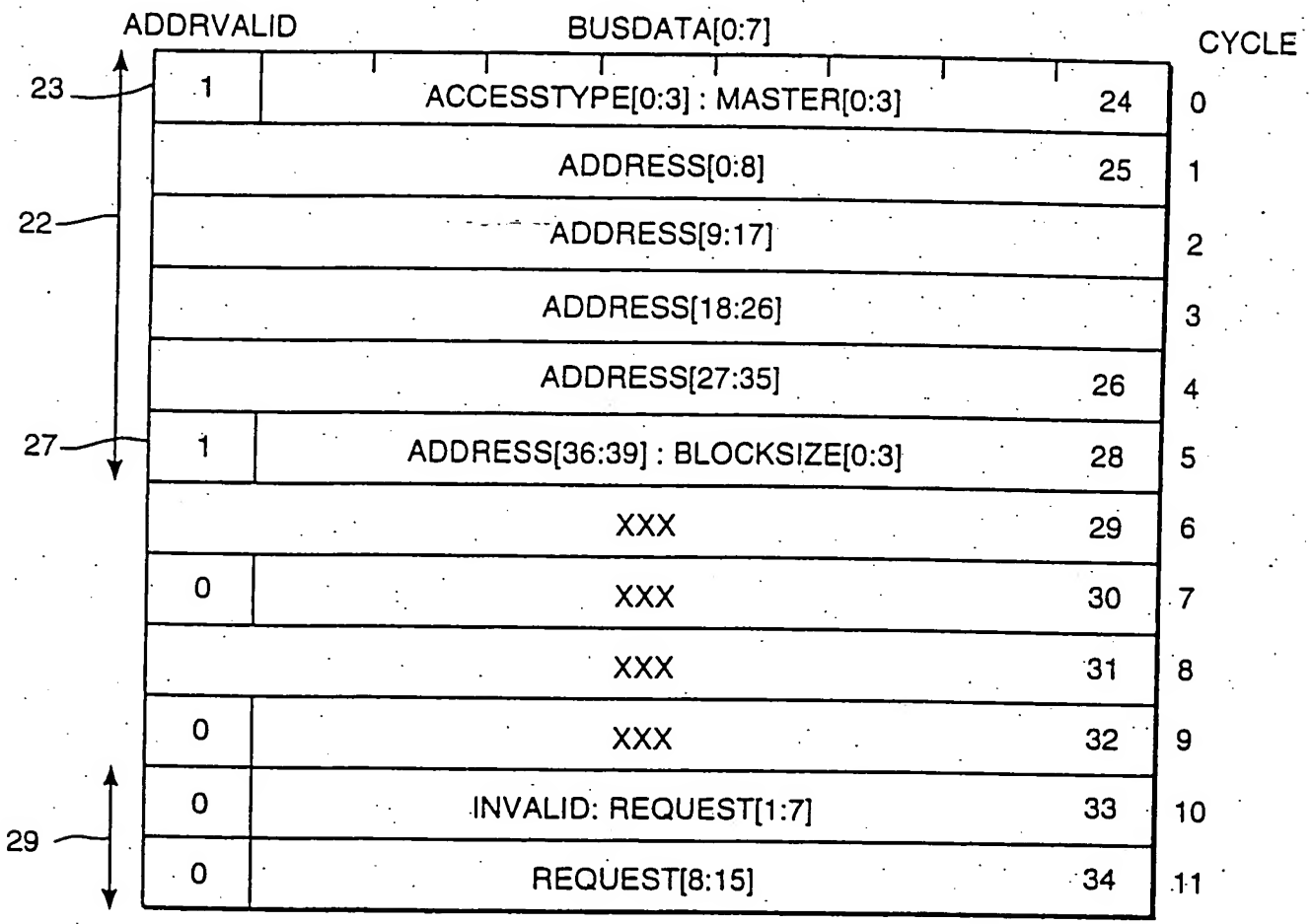


FIG_6

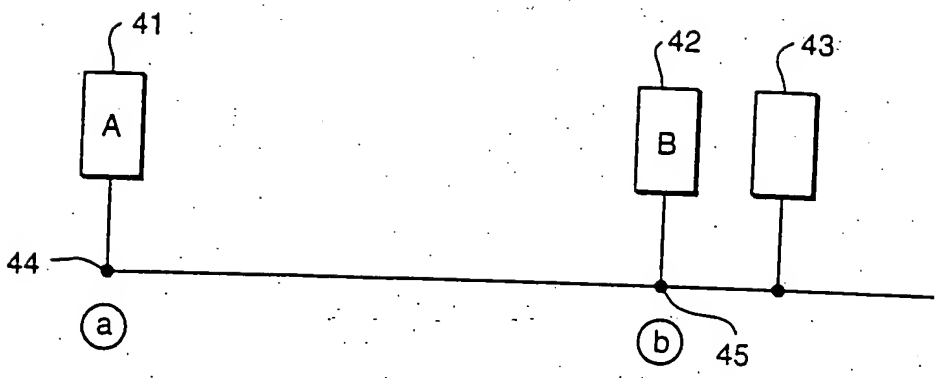


FIG_7A

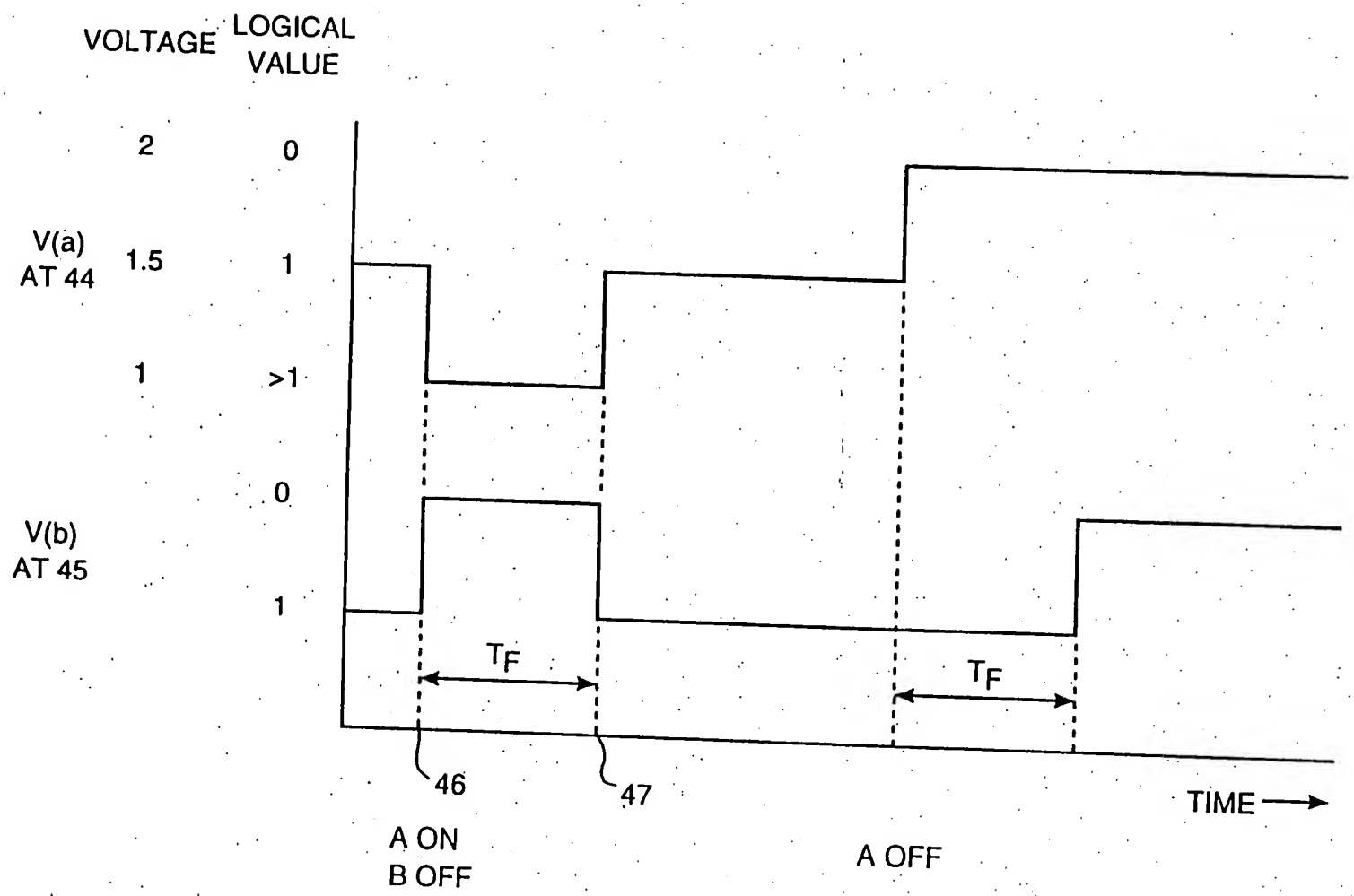

VOLTAGE
LOGICAL VALUE
2
0
V(a) AT 44
1.5
1
1
>1
0
V(b) AT 45
1
T_F
T_F
46
47
TIME
A ON
B OFF
A OFF

FIG_7B

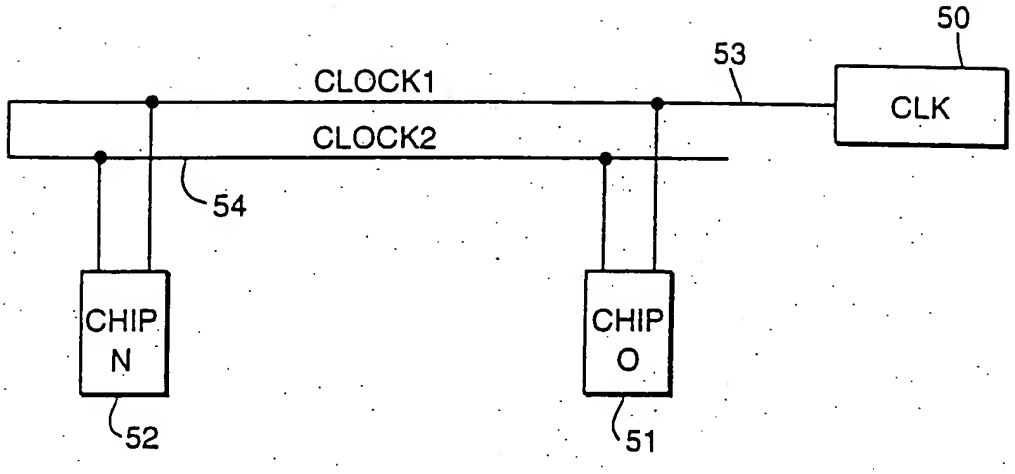

50
53
CLOCK1
CLK
CLOCK2
54
CHIP N
CHIP O
52
51

FIG_8A

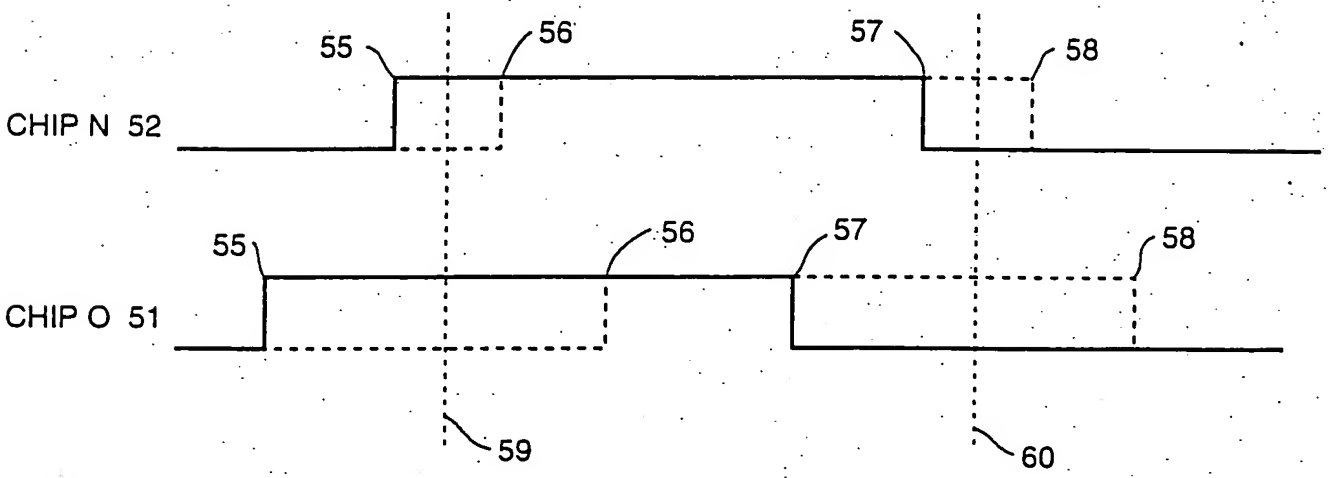
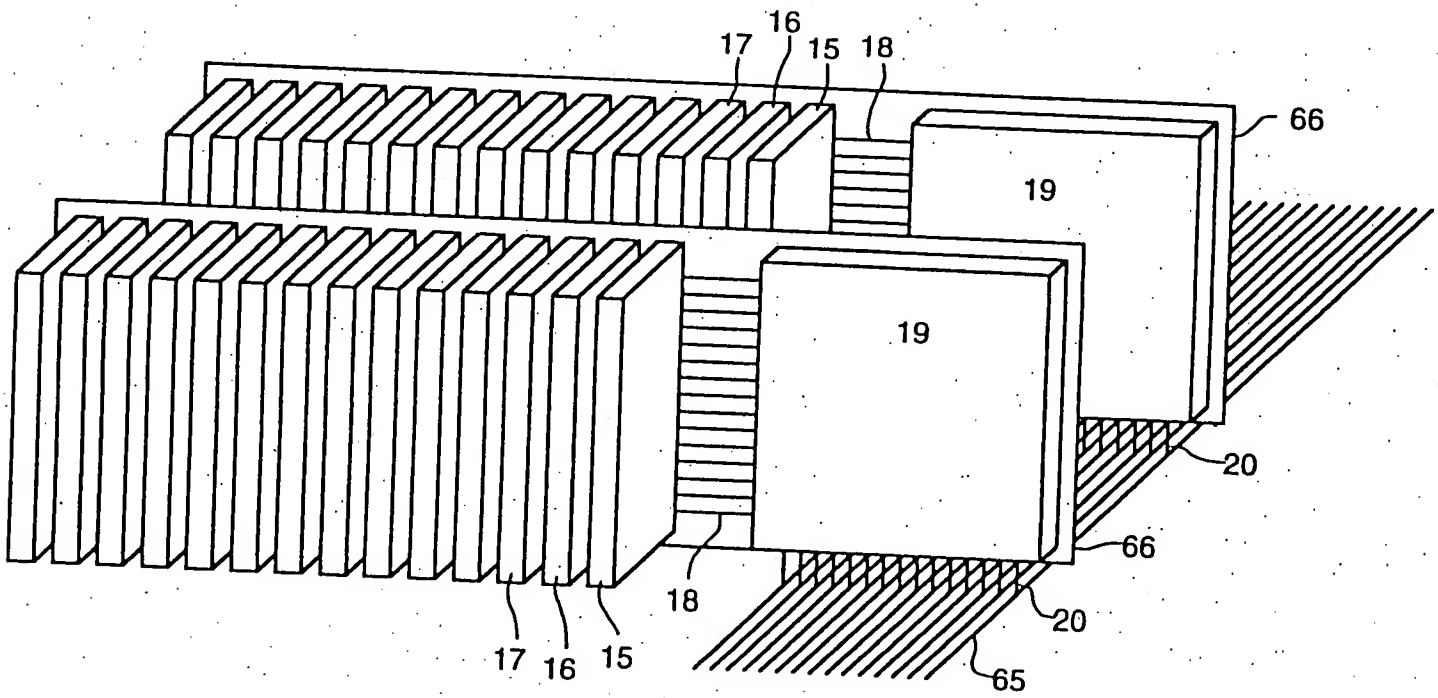

55
56
57
58
CHIP N 52
55
56
57
58
CHIP O 51
59
60

FIG_8B

FIG_9



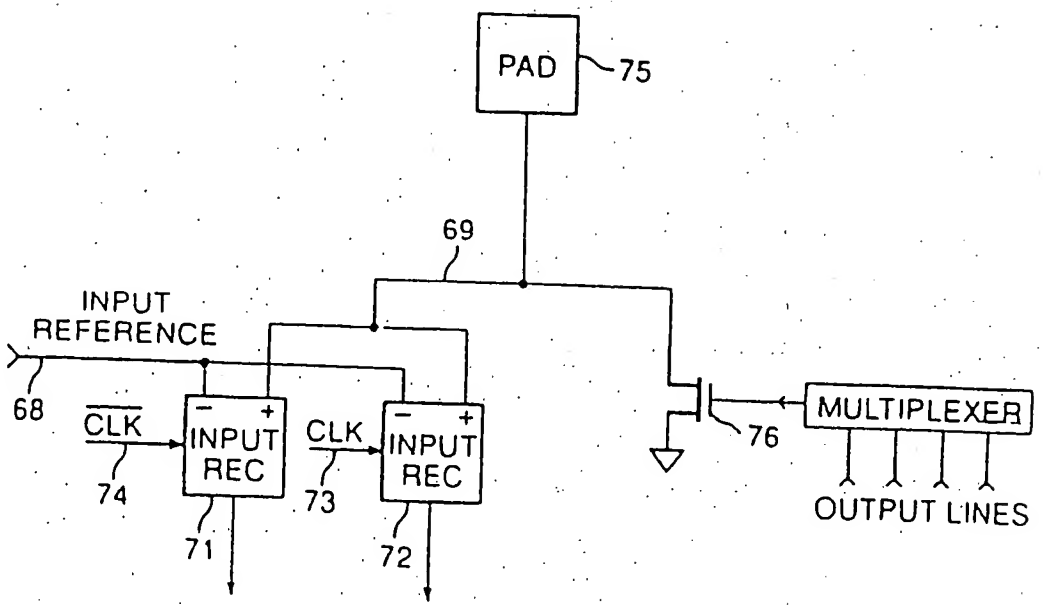

PAD
75
69
INPUT
REFERENCE
68
CLK
74
INPUT
REC
71
CLK
73
INPUT
REC
72
76
MULTIPLEXER
OUTPUT LINES

FIG. 10

FIG_11

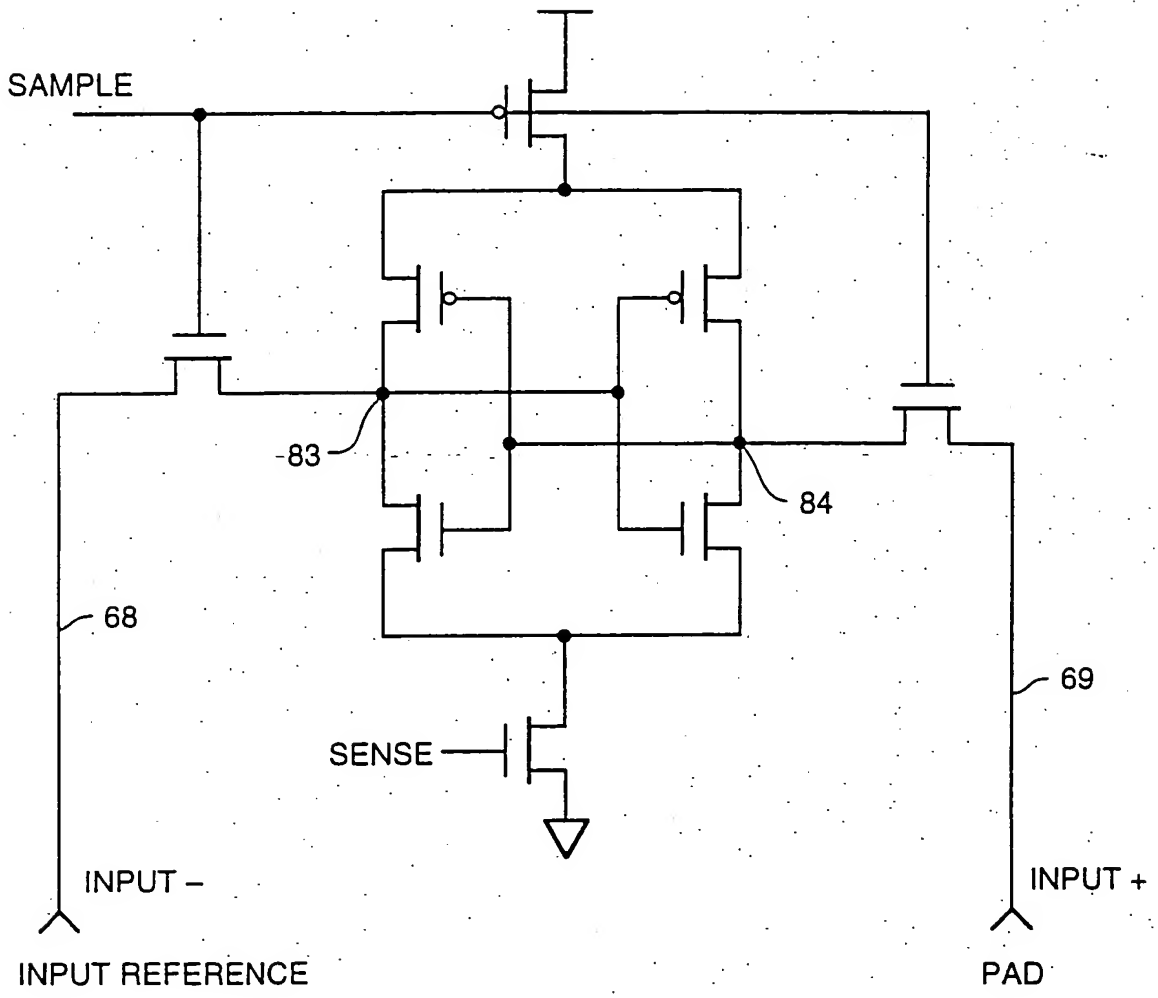


FIG_12

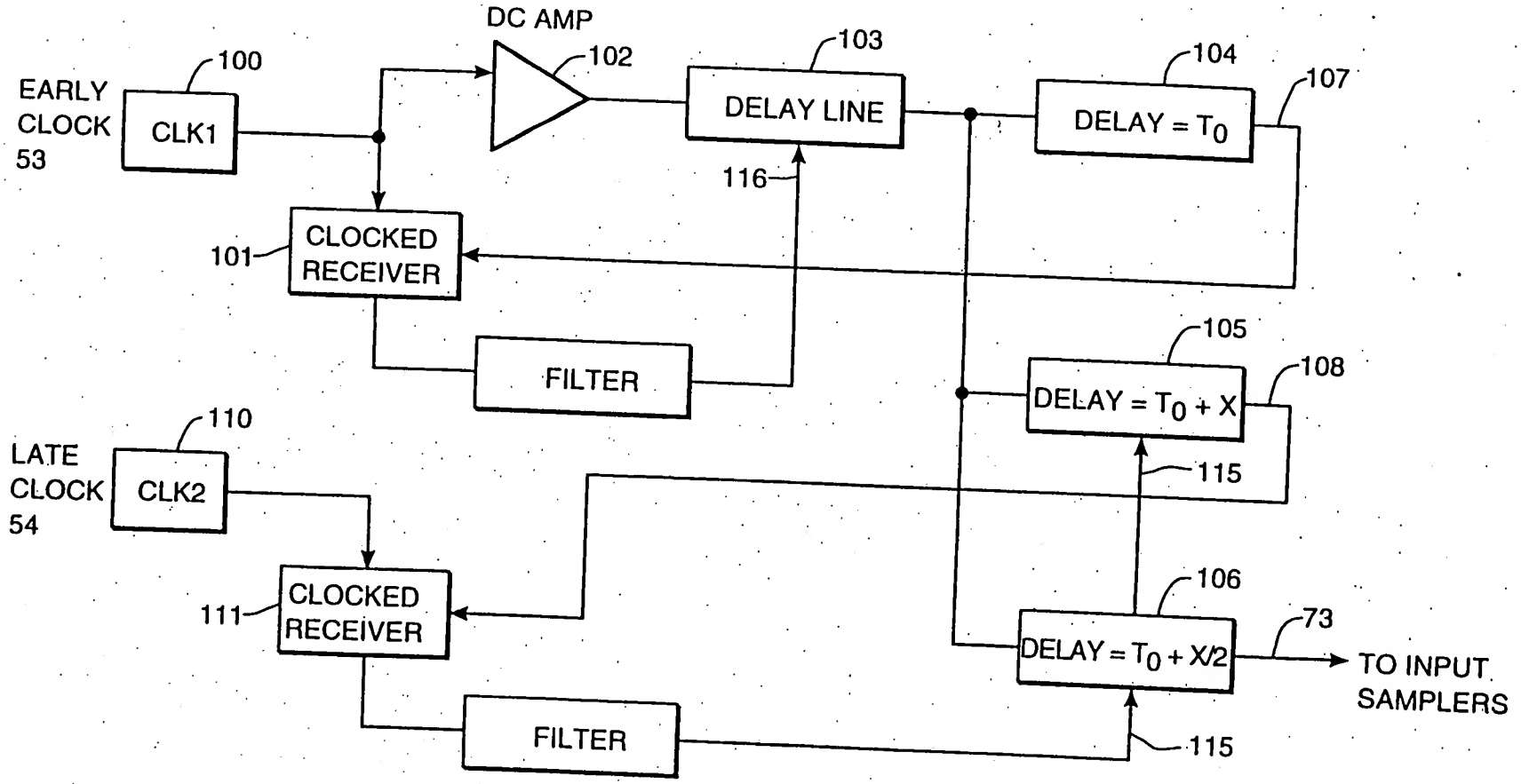
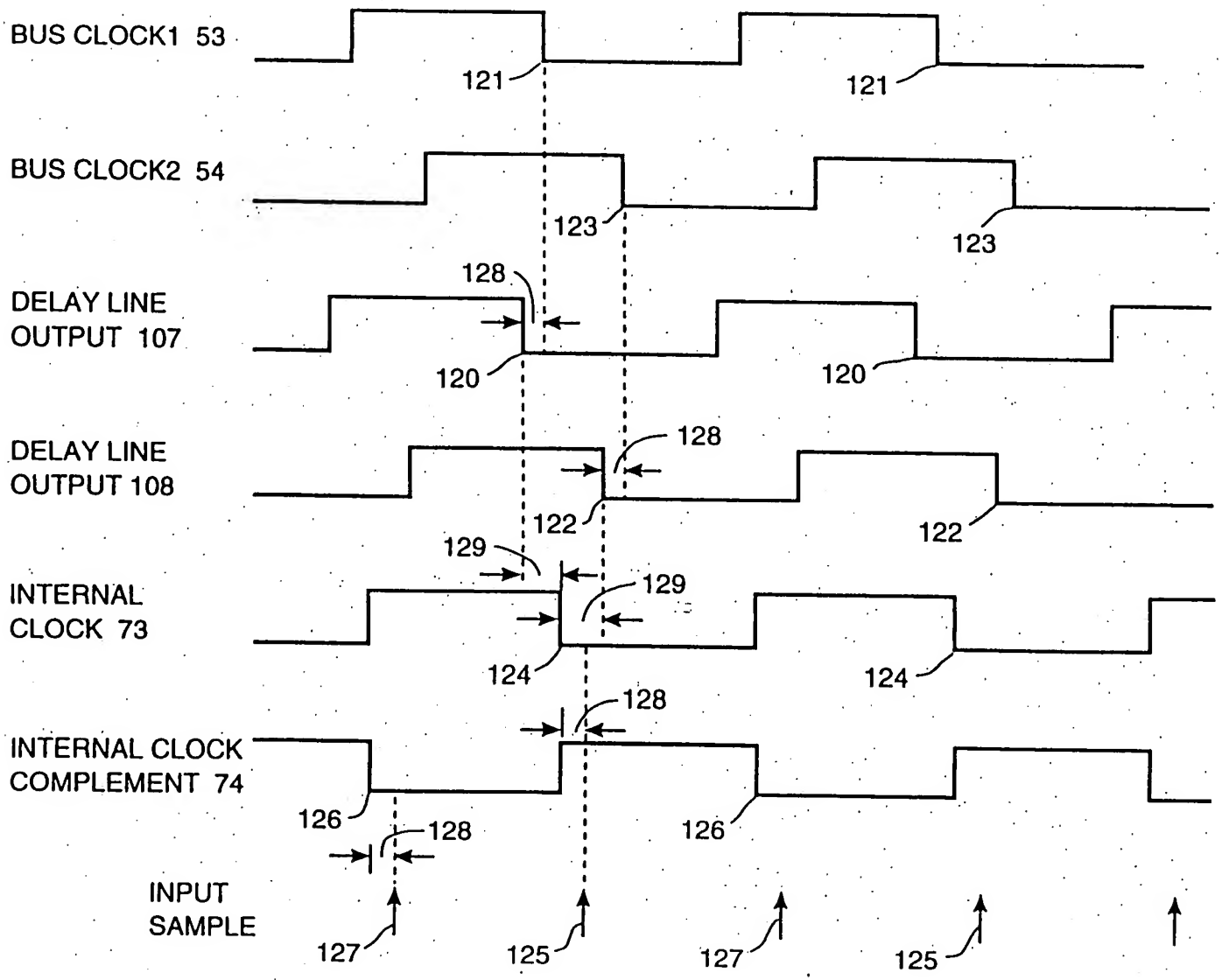

DC AMP
EARLY CLOCK 53
100
CLK1
102
103
DELAY LINE
104
DELAY = T_0
107
116
101
CLOCKED RECEIVER
FILTER
105
DELAY = T_0 + X
108
LATE CLOCK 54
110
CLK2
115
111
CLOCKED RECEIVER
106
DELAY = T_0 + X/2
73
TO INPUT SAMPLERS
FILTER
115

FIG_13


BUS CLOCK1 53
121
121
BUS CLOCK2 54
123
123
DELAY LINE OUTPUT 107
128
120
120
DELAY LINE OUTPUT 108
128
122
122
INTERNAL CLOCK 73
129
129
124
124
INTERNAL CLOCK COMPLEMENT 74
128
126
126
128
INPUT SAMPLE
127
125
127
125

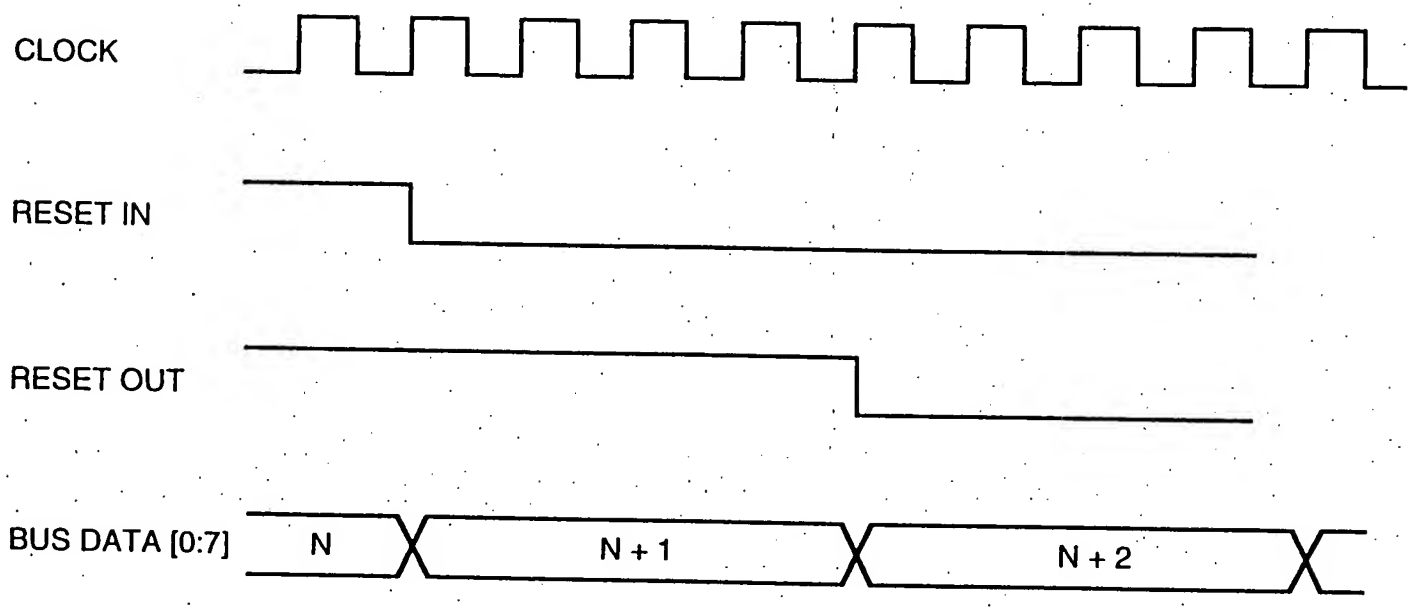
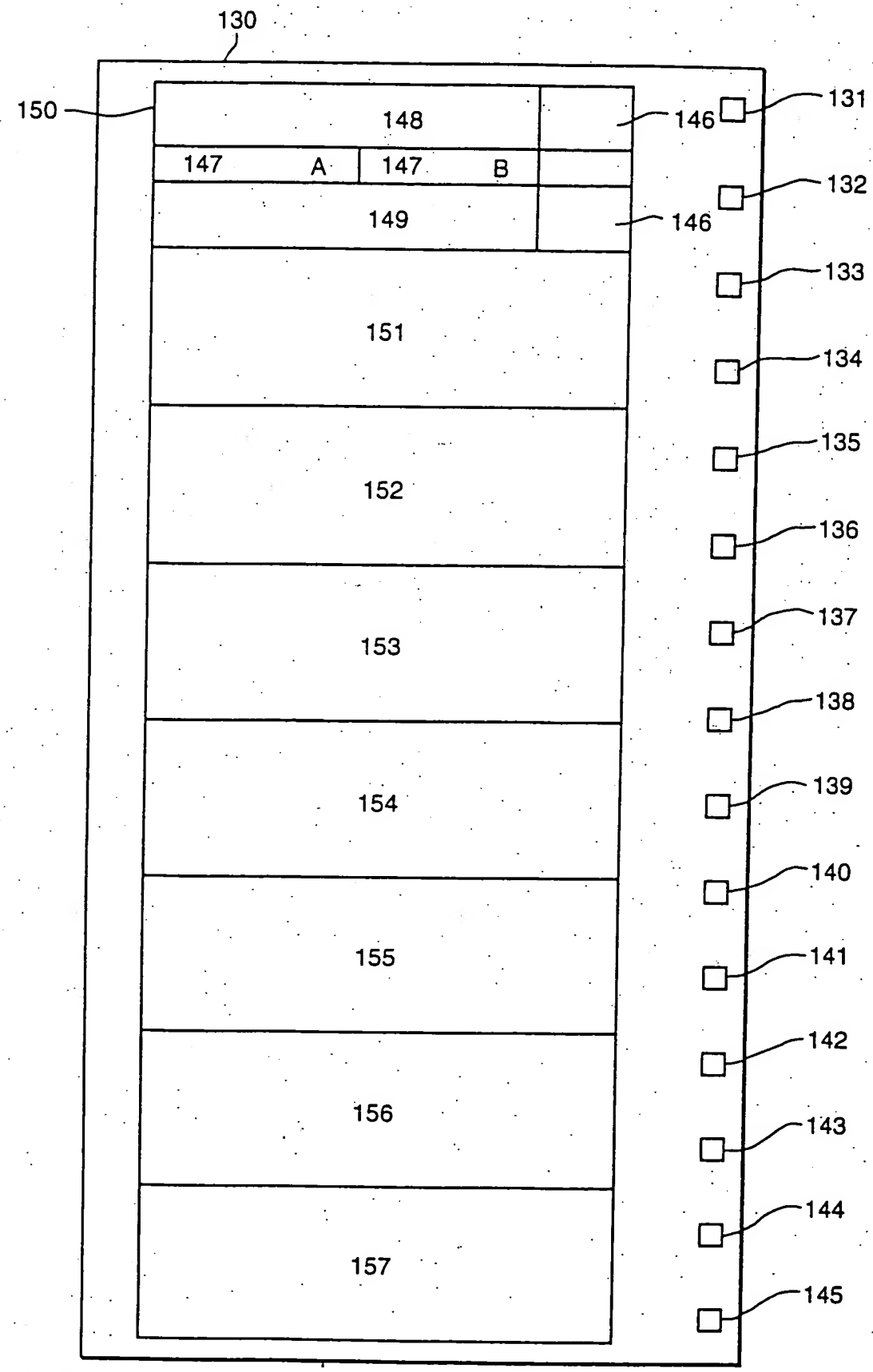


FIG_14

FIG_15


130
150
148
146
131
147 A
147 B
149
146
132
133
151
134
152
135
153
136
154
137
155
138
156
139
157
140
141
142
143
144
145